Amendment

Amendment to Claims

Please amend the claims as shown below.

5. (Once Amended) A method of forming a flash memory integrated circuit comprising:

forming a first and a second polysilicon/dielectric/polysilicon stack on a tunnel oxide of a substrate, wherein said first and second stacks are separated by a gap;

forming a shared source region in said gap between said first and said second polysilicon/dielectric/polysilicon stacks;

forming a first drain region adjacent to said first stack on the side opposite said shared source region;

forming a second drain region adjacent to said second stack on the side opposite said shared source region;

forming a dielectric layer over said first and said second stacks and over said first and said second drains wherein said dielectric layer completely fills said gap between said first and second stacks;

anisotropically [antisotropically] etching said dielectric layer from said first drain region and said second drain region so as to form a first spacer on the side of said first stack adjacent to said first drain and to form a second spacer on the side of said second stack adjacent to said second drain wherein in after said anisotropic [antisotropic] etch steps said gap remains filled with said dielectric.

7. (Once amended) A method of forming a flash memory integrated circuit comprising:

forming a first and a second polysilicon/dielectric/polysilicon stacks on a tunnel oxide formed on a silicon substrate, said first and said second stacks separated by a gap;

forming a shared source region in said silicon substrate in said gap and a first drain region adjacent to said first stack opposite said shared source region, and a second drain region adjacent to said second stack opposite said shared source;

forming a dielectric layer over said first drain over said first stack over said shared source, over said second stack, and over said second drain;

anisotropically [antisotropically] etching said dielectric to form spacer on said first drain adjacent to said first stack and a second spacer on said second drain adjacent to said second stack;

forming a metal film over said first drain, said first spacer, said first stack, said second stack, said second spacer, and said second drain; and

heating said substrate to cause said metal to react with said silicon in said first and said second drain regions and with said polysilicon of said first and second stacks to form a metal silicide on said first drain, said second drain, and on said top polysilicon of said first and second stacks.

Please add the following claims:

8. (Newly added) The method of claim 5, further comprising forming a trench in a dielectric material to form the gap.

9. (Newly added) A method of forming a non-volatile memory comprising:

forming a trench in a semiconductor substrate between a first cell and a second cell;

forming an opening in a first dielectric material in the trench;

forming a shared source region through the opening between the first cell and the second cell;

forming a second dielectric material in the opening in the first dielectric material; and

forming sidewall spacers with the second dielectric material.

10. (Newly added) The method of claim 9, further comprising growing a thermal oxide in the trench.

11. (Newly added) The method of claim 9, further comprising forming the second dielectric material with a chemical vapor deposition (CVD) process.

12. (Newly added) A non-volatile memory device comprising:

a first cell and a second cell formed over a semiconductor substrate, the substrate having a trench structure between the first cell and a second cell, wherein the trench structure has rounded corners;

a thermal oxide layer along at least a portion of the sides of the trench structure;

a dielectric material in the trench structure; and

a common source region in the semiconductor substrate and under at least a portion of an opening in the dielectric material.

13. (Newly added) The non-volatile memory device of claim 12, wherein the trench structure is aligned to sides of the first cell and the second cell.

14. (Newly added) The non-volatile memory device of claim 12, wherein the first cell and the second cell comprising an oxide/nitride/oxide dielectric stack.

CLEAN VERSION OF CLAIMS FOR SCANNING PER 37 CFR § 1.121

5. A method of forming a flash memory integrated circuit comprising:

forming a first and a second polysilicon/dielectric/polysilicon stack on a tunnel oxide of a substrate, wherein said first and second stacks are separated by a gap;

forming a shared source region in said gap between said first and said second polysilicon/dielectric/polysilicon stacks;

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forming a first drain region adjacent to said first stack on the side opposite said shared source region;

forming a second drain region adjacent to said second stack on the side opposite said shared source region;

forming a dielectric layer over said first and said second stacks and over said first and said second drains wherein said dielectric layer completely fills said gap between said first and second stacks;

anisotropically etching said dielectric layer from said first drain region and said second drain region so as to form a first spacer on the side of said first stack adjacent to said first drain and to form a second spacer on the side of said second stack adjacent to said second drain wherein in after said anisotropic etch steps said gap remains filled with said dielectric.

7. A method of forming a flash memory integrated circuit comprising:

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forming a first and a second polysilicon/dielectric/polysilicon stacks on a tunnel oxide formed on a silicon substrate, said first and said second stacks separated by a gap;

forming a shared source region in said silicon substrate in said gap and a first drain region adjacent to said first stack opposite said shared source region, and a second drain region adjacent to said second stack opposite said shared source;

forming a dielectric layer over said first drain over said first stack over said shared source, over said second stack, and over said second drain;

B2 anisotropically etching said dielectric to form spacer on said first drain adjacent to said first stack and a second spacer on said second drain adjacent to said second stack;

forming a metal film over said first drain, said first spacer, said first stack, said second stack, said second spacer, and said second drain; and

Concl'd heating said substrate to cause said metal to react with said silicon in said first and said second drain regions and with said polysilicon of said first and second stacks to form a metal silicide on said first drain, said second drain, and on said top polysilicon of said first and second stacks.

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8. The method of claim 5, further comprising forming a trench in a dielectric material to form the gap.

9. A method of forming a non-volatile memory comprising:

forming a trench in a semiconductor substrate between a first cell and a

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forming an opening in a first dielectric material in the trench;

forming a shared source region through the opening between the first cell and the second cell;

forming a second dielectric material in the opening in the first dielectric material; and

forming sidewall spacers with the second dielectric material.

10. The method of claim 9, further comprising growing a thermal oxide in the trench.

11. The method of claim 9, further comprising forming the second dielectric material with a chemical vapor deposition (CVD) process.

12. A non-volatile memory device comprising:

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a first cell and a second cell formed over a semiconductor substrate, the substrate having a trench structure between the first cell and a second cell, wherein the trench structure has rounded corners;

a thermal oxide layer along at least a portion of the sides of the trench structure;

a dielectric material in the trench structure; and

a common source region in the semiconductor substrate and under at least a portion of an opening in the dielectric material.

13. The non-volatile memory device of claim 12, wherein the trench structure is aligned to sides of the first cell and the second cell.

14. The non-volatile memory device of claim 12, wherein the first cell and the second cell comprising an oxide/nitride/oxide dielectric stack.